AMENDMENTS

Please amend the present application as follows:

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~---~~"), as is applicable:

1 - 11. (Canceled)

12. (Previously Presented) A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:

examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins;

determining that the first plurality of data units have a first compressibility characteristic; and

determining that the second plurality of data units have a second compressibility characteristic.

13. (Original) The method of claim 12, further comprising the step of: compressing the first plurality of data units independently from the second plurality of data units.

14. (Canceled)

15. (Original) The method of claim 12, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

16. (Original) The method of claim 12, wherein the first plurality of data units have a different timing complexity, a different vector data volume, and more repetitive data patterns than the second plurality of data units.

17 - 27. (Canceled)

28. (Previously Presented) A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:

memory configured to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins; and

a processor that is operative to:

determine that the first plurality of data units have a first compressibility characteristic;

determine that the second plurality of data units have a second compressibility characteristic.

29. (Original) The system of claim 28, wherein the processor is operative to:

compress the first plurality of data units independently from the second plurality of data units.

30. (Canceled)

31. (Original) The system of claim 28, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

32. (Original) The system of claim 28, wherein the first plurality of data units have a different timing complexity, a different vector data volume, and more repetitive data patterns than the second plurality of data unit